



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/891,999	06/26/2001	Ignacio A. Linares	1285-0053US	9611

24587 7590 03/26/2004

ALCATEL USA  
INTELLECTUAL PROPERTY DEPARTMENT  
3400 W. PLANO PARKWAY, MS LEGL2  
PLANO, TX 75075

EXAMINER

PHAN, RAYMOND NGAN

ART UNIT	PAPER NUMBER
----------	--------------

2111

DATE MAILED: 03/26/2004

3

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Applicati n N .

09/891,999

Applicant(s)

LINARES ET AL.

Examiner

Raymond Phan

Art Unit

2111

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-33 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-33 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.  
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).  
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_.
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_ 6) ☐ Other: \_\_\_\_.

### **Part III DETAILED ACTION**

#### ***Notice to Applicant(s)***

1. This application has been examined. Claims 1-33 are pending.
2. The Group and/or Art Unit location of your application in the PTO has changed. To aid in correlating any papers for this application, all further correspondence regarding this application should be directed to Group Art Unit 2111.

#### ***Specification***

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

#### ***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-5 are rejected under 35 U.S.C. § 102(b) as being anticipated by Cherukuri (US No. 5,878,217).

In regard to claim 1, Cherukuri discloses a network controller card (i.e. PC card) comprising a first interface controller 110 operable to be coupled to the first interface 114, the first interface operating to receive database input signals; a second interface controller 120 operable to be coupled to the second interface 118,

the second interface operating to couple the memory card to the bus (see figure 1, col. 6, line 33 through col. 7, line 39); a first memory interface disposed between the first interface controller and the memory block 102 (see figure 1, col. 3, line 15 through col. 4, line 39); a second memory interface disposed between the second interface controller and the memory block (see figure 1, col. 3, line 15 through col. 4, line 39); a buffer resource manager 210 arbitrates between requests for read access buffer by the host interface 204 and by DMA controller 206 as well as write access to store data frames received in the memory buffer 202 (see figure 2, col. 4, lines 33-39).

In regard to claim 2, Cherukuri discloses wherein the first interface comprising a network interface coupled to the switch fabric disposed in the telecommunications node (see col. 3, lines 15-35).

In regard to claim 3, Cherukuri discloses wherein the switch fabric comprising an Ethernet fabric (see col. 3, lines 15-35).

In regard to claim 4, Cherukuri discloses the error correction module coupled to the buffer (see col. 3, lines 15-35).

In regard to claim 5, Cherukuri disclose the synchronous logic responsive to a data synchronous signal, to synchronize the data input operations with respect to the buffer with data input operation associated with the network card (see col. 4, lines 40-53).

### ***Claim Rejections - 35 USC § 103***

6. The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 6-8 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Cherukuri in view of Matsushima et al. (US No. 5,706,482).

In regard to claim 6, Cherukuri discloses the claimed subject matter as discussed above rejection except the teaching of wherein the memory block comprising at least one DRAM module. However Matsushima et al. disclose wherein the memory block comprising at least one DRAM module (see col. 2, lines 43-54). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Matsushima et al. within the system of Cherukuri et al. because it would allow the continuously flowing of data (i.e. written or/and read) between devices.

In regard to claim 7, Matsushima et al. disclose wherein the memory block comprising at least one SDRAM module (see col. 5, lines 56-61). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Matsushima et al. within the system of Cherukuri et al. because it would allow the continuously flowing of data (i.e. written or/and read) between devices.

In regard to claim 8, Cherukuri discloses wherein the memory block comprising at least one high-speed, high density NVM (i.e. buffer) module (see col. 3, lines 15-35).

8. Claims 9-11 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Cherukuri in view of Matsushima et al. and Lanus et al. (US No. 6,112,271).

In regard to claims 9-10, Cherukuri and Matsushima et al. disclose the claimed subject matter as discussed above rejection except the teaching of wherein the bus comprising a system bus operating to interconnect a plurality of processor

cards disposed in a system shelf. However Lanus et al. disclose the multiconfiguration backplane has compact PCI 110 operable for connecting the plurality of processor boards (see col. 3, lines 38-55). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Lanus et al. within the system of Cherukuri and Matsushima et al. because it would provide a single backplane with multiple configuration.

In regard to claim 11, Lanus et al. disclose wherein the system shelf forming at least a portion of a telecommunications node (see col. 5, lines 36-59). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Lanus et al. within the system of Cherukuri and Matsushima et al. because it would provide a single backplane with multiple configuration.

9. Claims 12-16, 20-21, 24-26, 32-33 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Velamnuri et al. (US No. 6,286,011) in view of Cherukuri.

In regard to claims 12, 24, Velamnuri et al. disclose a system for updating a distributed database associated with a telecommunications node comprising a database update manager for generating an update signal indicative at least of updated data (see col. 8, lines 18-44). But Velamnuri et al. do not disclose at least memory card disposed in the system shelf forming a portion of the telecommunication node, the memory card cooperating with the network interface for receiving the database signal through the switch fabric, wherein the memory card is operable to contain at least a portion of the distributed database in the memory block disposed thereon. However Cherukuri discloses a network

controller card (i.e. PC card) comprising a first interface controller 110 operable to be coupled to the first interface 114, the first interface operating to receive database input signals; a second interface controller 120 operable to be coupled to the second interface 118, the second interface operating to couple the memory card to the bus (see figure 1, col. 6, line 33 through col. 7, line 39); a first memory interface disposed between the first interface controller and the memory block 102 (see figure 1, col. 3, line 15 through col. 4, line 39); a second memory interface disposed between the second interface controller and the memory block (see figure 1, col. 3, line 15 through col. 4, line 39). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Cherukuri within the system of Velamnuri et al. because it would provide an easy and portable access to the database system.

In regard to claims 13-14, 26, Cherukuri disclose the synchronous logic responsive to a data synchronous signal, to synchronize the data input operations with respect to the buffer with data input operation associated with the network card (see col. 4, lines 40-53). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Cherukuri within the system of Velamnuri et al. because it would provide an easy and portable access to the database system.

In regard to claim 15, Velamnuri et al. disclose the database manager is co-located with the telecommunications node (see 6, lines 31-65).

In regard to claims 16, 25, Cherukuri discloses wherein the switch fabric comprising an Ethernet fabric (see col. 3, lines 15-35). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was

made to have combined the teachings of Cherukuri within the system of Velamnuri et al. because it would provide an easy and portable access to the database system.

In regard to claims 20, 33, Cherukuri discloses a network controller card (i.e. PC card) comprising a first interface controller 110 operable to be coupled to the first interface 114, the first interface operating to receive database input signals; a second interface controller 120 operable to be coupled to the second interface 118, the second interface operating to couple the memory card to the bus (see figure 1, col. 6, line 33 through col. 7, line 39); a first memory interface disposed between the first interface controller and the memory block 102 (see figure 1, col. 3, line 15 through col. 4, line 39); a second memory interface disposed between the second interface controller and the memory block (see figure 1, col. 3, line 15 through col. 4, line 39); a buffer resource manager 210 arbitrates between requests for read access buffer by the host interface 204 and by DMA controller 206 as well as write access to store data frames received in the memory buffer 202 (see figure 2, col. 4, lines 33-39). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Cherukuri within the system of Velamnuri et al. because it would provide an easy and portable access to the database system.

In regard to claim 21, 32, Cherukuri discloses the error correction module coupled to the buffer (see col. 3, lines 15-35). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Cherukuri within the system of Velamnuri et al. because it would provide an easy and portable access to the database system.

10. Claims 17-19, 27-29 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Velamnuri et al. in view of Cherukuri and further in view of Matsushima et al.

In regard to claims 17, 27, Cherukuri discloses the claimed subject matter as discussed above rejection except the teaching of wherein the memory block comprising at least one DRAM module. However Matsushima et al. disclose wherein the memory block comprising at least one DRAM module (see col. 2, lines 43-54). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Matsushima et al. within the system of Cherukuri et al. because it would allow the continuously flowing of data (i.e. written or/and read) between devices.

In regard to claim 18, 28, Matsushima et al. disclose wherein the memory block comprising at least one SDRAM module (see col. 5, lines 56-61). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Matsushima et al. within the system of Cherukuri et al. because it would allow the continuously flowing of data (i.e. written or/and read) between devices.

In regard to claim 19, 29, Cherukuri discloses wherein the memory block comprising at least one high-speed, high density NVM (i.e. buffer) module (see col. 3, lines 15-35).

11. Claims 21-23, 30-31 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Velamnuri et al. in view of Cherukuri and further in view of Lanus et al.

In regard to claims 21, 23, 30-31, Cherukuri and Matsushima et al. disclose the claimed subject matter as discussed above rejection except the teaching of wherein the bus comprising a system bus operating to interconnect a plurality of processor cards disposed in a system shelf. However Lanus et al. disclose the multiconfiguration backplane has compact PCI 110 operable for connecting the plurality of processor boards (see col. 3, lines 38-55). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Lanus et al. within the system of Cherukuri and Matsushima et al. because it would provide a single backplane with multiple configuration.

In regard to claim 22, Lanus et al. disclose wherein the system shelf forming at least a portion of a telecommunications node (see col. 5, lines 36-59). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Lanus et al. within the system of Cherukuri and Matsushima et al. because it would provide a single backplane with multiple configuration.

### ***Conclusion***

12. All claims are rejected.

13. The prior arts made of record and not relied upon are considered pertinent to applicant's disclosure.

**Nattkemper et al. (US No. 5,999,518)** disclose a distributed telecommunications switching system and method.

Art Unit: 2111

**Burton et al. (US No. 6,526,419)** disclose a method, system and program for remote copy in an open systems environment.

**Singh et al. (US No. 5,758,083)** disclose a method and system for sharing information between network managers.

**Terasaki et al. (US No. 6,292,863)** disclose a PC card.

**Oh-Yang et al. (US No. 6,351,820)** disclose a PC card with automated drag and sleep function.

**Chaco (US No. 5,465,082)** discloses an apparatus for automating routine communication in a facility.

**Le Roux (US No. 5,802,325)** discloses a mass memory card with input/output function.

**Seguchi (US Pub No. 2001/0007123)** discloses a stored program controlled switch system.

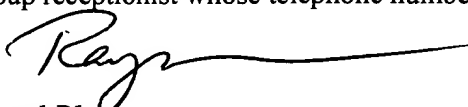
14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Raymond Phan, whose telephone number is (703) 306-2756. The examiner can normally be reached on Monday-Friday from 6:30AM- 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's Primary, Paul Myers can be reached on (703) 305-9656 or via e-mail addressed to paul.myers@uspto.gov. The fax phone number for this Group is (703) 872-9306.

Communications via Internet e-mail regarding this application, other than those under 35 U.S.C. 132 or which otherwise require a signature, may be used by the applicant and should be addressed to [raymond.phan@uspto.gov].

All Internet e-mail communications will be made of record in the application file. PTO employees do not engage in Internet communications where there exists a possibility that sensitive information could be identified or exchanged unless the record includes a properly signed express waiver of the confidentiality requirements of 35 U.S.C. 122. This is more clearly set forth in the Interim Internet Usage Policy published in the Official Gazette of the Patent and Trademark on February 25, 1997 at 1195 OG 89.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.



**Raymond Phan**

3/13/04